DataGeneral

TECHNICAL STATEMENT

TEXT LISTING

068-000540-01

PROGRAM

MICRO NOVA DIGITAL TO ANALOG
INTERFACE DIAGNOSTIC

TEXT TAPE

097-000540-01

ABSTRACT

THIS PROGRAM IS A LOGIC LEVEL TEST OF THE MODEL 4224 MICRO NOVA DIGITAL TO ANALOG INTERFACE.

COPYRIGHT © DATA GENERAL CORPORATION, 1978
ALL RIGHTS RESERVED. PRINTED IN U.S.A.

```
 0001 .MAIN     MACRO REV 06.30          13:20:28 08/10/78
01
02
03
04              ;*************************************************************
05              ;
06              ; NAME: MNDAC.TX                          PART NUMBER: 097-000540
07              ;
08              ;
09              ; DESCRIPTION: MICRO NOVA DIGITAL TO ANALOG INTERFACE DIAGNOSTIC
10              ;
11              ;
12              ; REVISION HISTORY:
13              ;
14              ;       REV.            DATE
15              ;
16              ;       00              10/21/77
17              ;       01              08/10/78
18              ;
19              ;
20              ; COPYRIGHT (C) DATA GENERAL CORPORATION, 1977, 1978
21              ; ALL RIGHTS RESERVED.
22              ; LICENSED MATERIAL - PROPERTY OF DATA GENERAL CORPORATION.
23              ;*************************************************************
```

```
 0002 .MAIN
01              ;1.     PROGRAM NAME:
02              ;       ============
03              ;       MNDAC   -   MICRO NOVA DIGITAL TO ANALOG INTERFACE
04              ;                               DIAGNOSTIC
05
06              ;2.     REVISION HISTORY:
07              ;       =================
08              ;       REV 00   -   10/21/77
09              ;       REV 01   -   08/10/78
10
11              ;3.     MACHINE REQUIREMENTS:
12              ;       =====================
13              ;       1.  MICRO NOVA CENTRAL PROCESSOR WITH AT LEAST
14              ;           4K READ/WRITE (RAM) MEMORY
15              ;       2.  MICRO NOVA ASYNCHRONOUS INTERFACE
16              ;       3.  TELETYPE OR CRT TERMINAL
17              ;       4.  PAPER TAPE READER AND/OR DISKETTE DRIVE
18
19              ;4.     TEST REQUIREMENTS:
20              ;       ==================
21              ;       1.  MICRO NOVA DIGITAL TO ANALOG INTERFACE MODEL 4224
22              ;       2.  MICRO NOVA DIGITAL TO ANALOG INTERFACE DIAGNOSTIC
23              ;           - AB TAPE PART # 095 - 000540
24              ;             LISTING PART # 096 - 000540
25              ;       3.  ONE OF THE FOLLOWING D/A INTERFACE JUMPERS MUST
26              ;           BE INSERTED TO ALLOW Z-AXIS PULSE TRIGGERING:
27              ;           - CLOCK X (JUMPER M22) OR
28              ;             CLOCK Y (JUMPER M21)
29
30              ;5.     SUMMARY:
31              ;       =======
32              ;       THIS PROGRAM IS A LOGIC LEVEL TEST OF THE MODEL 4224
33              ;       MICRO NOVA DIGITAL TO ANALOG INTERFACE.
```

```
;6.     RESTRICTIONS:
;       ============
;       1.  THIS DIAGNOSTIC CAN TEST ONE D/A INTERFACE
;           AT A TIME.
;       2.  ALL DEVICES CONNECTED TO THE D/A INTERFACE SHOLUD
;           BE DISCONNECTED DURING DIAGNOSTIC TESTING.
;       3.  THE FOLLOWING ANALOG SIGNALS ARE NOT TESTED
;           BY THIS DIAGNOSTIC AS THEY ARE OUTPUT ONLY
;           FUNCTIONS; ERASE, ZERODAC (0EX/0EY), DAC DATA
;           VALID, WRITE THROLGH, DAC X OUT, DAC Y OUT,
;           Z-AXIS OUT, TC1, TC2, OB1, OB2, BRTXMSB,
;           BRTYMSB, BRTXLSB, BRTYLSB, X & Y DATA
;           REGISTERS (ALTHOUGH DATA IS OUTPUT TO THEM),
;           DAC DATA READY AND INTERNAL CLOCK (HAND-
;           SHAKING SIGNALS ONLY).

;           THESE FUNCTIONS/SIGNALS ARE EXERCISED IS THE
;           "MICRO NOVA DIGITAL TO ANALOG EXERCISER",
;            - AB TAPE PART # 095 - 0000638
;              LISTING PART # 096 - 0000638

;           THIS INTERFACE CAN ALSO BE TESTED ON A SYSTEMS
;           LEVEL BY USING "MICRO NOVA ANALOG CONVERSION
;           SYSTEM EXERCISER",
;           - AB TAPE PART # 095 - 0001059
;           - LISTING PART # 096 - 0001059

;       4.  ALL DEVICES CONNECTED TO THE D/A ANLAOG
;           OUTPUTS SHOULD BE DISCONNECTED DURING
;           DIAGNOSTIC TESTING.
```



```
;7.     PROGRAM DESCRIPTION/THEORY OF OPERATION:
;       ========================================
;       NOTE: THE FOLLOWING CONVENTION IS USED IN THE
;             DESCRIPTION TO INDICATE LOW ACTIVE SIGNALS:

;                          ==========
;                 /SIGNALNAME/ = SIGNALNAME

;7.1    DIGITAL TO ANALOG CONVERTER OPERATION:
;       THE D/A INTERFACE FOR THE MICRO NOVA CONSISTS OF
;       TWO 12-BIT HYBRID D/A CONVERTERS WITH SCOPE CONTROL,
;       LOGIC AND INTERFACE CIRCUITRY. VOLTAGE RANGES FOR
;       THE DACS (JUMPER SELECTABLE) ARE 0-5, 0-10,
;       +/- 5, +/- 10 VOLTS DC. THE VOLTAGE RANGES OF THE TWO
;       DACS ARE INDEPENDENT OF EACH OTHER. MAXIMUM SETTLING
;       TIME TO 0.01% OF FULL SCALE READING IS TYPICALLY 7 US.
;       LINEARITY AND DIFFERENTIAL LINEARITY ARE EACH +/-
;       1/2 LSB AND CONVERSION IS MONOTONIC. EACH DAC HAS
;       AN OUTPUT AMPLIFIER ENABLING IT TO DRIVE 5 MA LOADS.
;       AN ON BOARD DC-DC CONVERTER PROVIDES THE +/- 15 VDC
;       NECESSARY FOR THE ANALOG CIRCUITRY. CODING FOR THE
;       CONVERTERS (JUMPER SELECTABLE) IS EITHER OFFSET BINARY
;       OR TWO'S COMPLEMENT.

;       A DOUBLE BUFFERING SCHEME ALLOWS SYNCHRONIZATION OF
;       OUTPUT DATA TO THE D/A CONVERTERS WITH EITHER AN
;       INTERNAL OR EXTERNAL CLOCK. THE FIRST BUFFER IS LOADED
;       BY A DOC INSTRUCTION FOR PROGRAMMED I/O (PIO) OR
;       /DCHO/ FOR DATA CHANNEL (DCH) CONVERSIONS. AT THIS
;       POINT, BOTH THE DAC DATA READY STATUS BIT
;       (READABLE BY A DIA INSTRUCTION) AND OUTPUT SIGNAL
;       (JUMPER SELECTABLE ACTIVE HIGH OR LOW) BECOME ACTIVE.
;       THEY REMAIN ACTIVE UNTIL A CLOCK SIGNAL OCCURS TO
;       LOAD THE SECOND BUFFER WHICH SENDS THE DATA TO
;       ONE OF THE DACS FOR CONVERSION TO ITS EQUIVALENT
;       ANALOG VOLTAGE OUTPUT. APPROXIMATELY 7 US LATER,
;       AFTER THE DAC HAS SETTLED TO ITS NEW VALUE, THE DAC
;       DATA VALID OUTPUT SIGNAL BECOMES ACTIVE (ALSO JUMPER
;       SELECTABLE ACTIVE HIGH OR LOW) AND REMAINS ACTIVE
;       UNTIL THE NEXT CONVERSION IS STARTED.

;       THERE ARE SEVEN DIFFERENT CLOCK SOURCES FOR SENDING
;       DATA TO THE DACS. FOR PROGRAMMED I/O (PIO) THEY ARE:
;       /STRT/ - NO CLOCK SYNCRONIZATION, INTERNAL CLOCK
;       SYNCHRONIZATION, EXTERNAL CLOCK SYNCHRONIZATION.
;       FOR DATA CHANNEL (DCH) TRANSFERS THEY ARE: /IOPLS/
;       (ONE CONVERSION FOR EVERY /IOPLS/ ISSUED TO THE D/A),
;       DATA READY (OCCURS ONE FSTROBE AFTER /DCHO/ AND
;       REPRESENTS THE MAXIMUM TRANSFER RATE), INTERNAL
;       CLOCK SYNCRONIZATION, EXTERNAL SYNCHRONIZATION.
;       FOR /IOPLS/ DCH TRANSFERS, THE TIME BETWEEN
;       SUBSEQUENT IOPLS'S SHOULD BE GREATER THAN THE
;       MAXIMUM DATA CHANNEL LATENCY. ALSO, AN I/O
;       INSTRUCTION WITH AN IOPLS APPENDED (I.E. NIOP)
;       SHOULD NOT BE GIVEN TO THE D/A UNTIL DATA READY
;       IS ACTIVE (DATA LOADED INTO FIRST BUFFER). THIS
;       CAN BE CHECKED BY READING THE D/A STATUS (DIA).
```

```
|0005 .MAIN
01                  ;       IF AN EXTERNAL CLOCK IS USED, THE CLOCK SIGNAL
02                  ;       MUST BE HIGH FOR AT LEAST 2 US AND LOW FOR AT
03                  ;       LEAST 2 US AND HAVE A PERIOD GREATER THAN THE
04                  ;       SETTLING TIME OF THE DACS (7 US TYPICAL),
05                  ;       AND FOR DATA CHANNEL TRANSFERS, HAVE A PERIOD
06                  ;       GREATER THAN THE MAXIMUM DATA CHANNEL LATENCY.
07
08                  ;       THE CLOCK SOURCE IS SELECTED BY THREE STATUS BITS
09                  ;       IN A DOA INSTRUCTION. THE DOA INSTRUCTION ALSO
10                  ;       CONTAINS AN ALTERNATE BIT, WHICH IS SET TO INDICATE
11                  ;       ALTERNATING CONVERSIONS BETWEEN THE TWO DACS, A DAC
12                  ;       SELECT BIT TO SELECT WHICH DAC RECEIVES THE FIRST
13                  ;       DATA AND FOUR SELECTABLE SCOPE FUNTION BITS. THEY
14                  ;       ARE /SCOPE MODE/, /NON-STORE/, /WRITE-THROUGH/
15                  ;       AND /ERASE/. THE ERASE STATUS BIT CAUSES A PULSE
16                  ;       OF DURATION APPROXIMATELY 2 MS ON THE /ERASE/ LINE
17                  ;       (A13, LOW ACTIVE OPEN COLLECTOR SIGNAL), WHICH CAN BE
18                  ;       USED TO ERASE A SCOPE. THE DOA COMMAND SHOULD NOT
19                  ;       BE GIVEN IF BUSY IS SET AND MUST APPEAR FIRST BEFORE
20                  ;       DOB AND DOC IN A DATA CHANNEL SETUP SEQUENCE. ALL
21                  ;       STATUS BITS REMAIN THE SAME UNTIL THE NEXT DOA
22                  ;       INSTRUCTION OR /IORST/, WHICH CLEARS ALL STATUS BITS.
23                  ;       SYNCHRONIZTION TO A CLOCK OCCURS ON THE FALLING
24                  ;       EDGE OF THE CLOCK.
25
26                  ;       WHEN POWER IS FIRST APPLIED TO THE DAC BOARD
27                  ;       THE DIGITAL CODE FOR 0 VOLTS IS APPLIED TO EACH DAC
28                  ;       UNTIL THE FIRST CONVERSION. /IORST/ AGAIN CAUSES 0
29                  ;       VOLTS TO BE OUTPUTTED FROM EACH DAC. OTHERWISE, THE
30                  ;       VOLTAGE OUTPUT OF EACH DAC IS THAT OF THE LAST
31                  ;       CONVERSION.
32
33                  ;       IF THE /SCOPE MODE/ IN A DOA INSTRUCTION (D4) IS 0
34                  ;       (ACTIVE LOW SIGNAL), A Z-AXIS PULSE WILL OCCUR EVERY
35                  ;       TIME A NEW DIGITAL CODE IS SENT TO EITHER DAC X
36                  ;       OR DAC Y (JUMPER SELECTABLE). THE Z PULSE,
37                  ;       WHICH IS AN INTENSIFICATION PULSE, ACTUALLY OCCURS
38                  ;       AFTER A 7 US DELAY TO ALLOW DAC SETTLING.
39                  ;       THE Z PULSE MAY BE AC OR DC COUPLED (JUMPER
40                  ;       SELECTABLE). THE DC LEVEL OF THE Z-AXIS SIGNAL
41                  ;       SHOULD BE ADJUSTED BY THE POT PROVIDED SO THAT
42                  ;       THE CRT OR OSCILLOSCOPE TRACE IS JUST BARELY
43                  ;       BLANKED. THE Z PULSE CAN BE UP TO THREE 0.5
44                  ;       VOLT LEVELS ABOVE OR BELOW THIS DC LEVEL (UP-DOWN
45                  ;       IS JUMPER SELECTABLE). THE AMPLITUDE OF THE Z
46                  ;       PULSE CAN BE INCREASED TO THREE 2 VOLT LEVELS
47                  ;       BY CHANGING THE 3.3K RESISTOR TO 680 OHMS AND
48                  ;       THE 6.2K TO 3.3K. THE BRIGHTNESS OF THE Z PULSE
49                  ;       IS DETERMINED BY BITS 14 AND 15 OF THE DATA WORD
50                  ;       WHICH CAUSES THE Z PULSE (NOTE THAT BITS 0-11
51                  ;       CONTAIN D/A DATA). THE FOLLOWING CODES DETERMINE
52                  ;       THE BRIGHTNESS:
53
54                  ;       D14     D15             BRIGHTNESS LEVEL
55                  ;       0       0       1.5 VOLTS +/- DC LEVEL
56                  ;       0       1       1.0 VOLTS +/- DC LEVEL
57                  ;       1       0       0.5 VOLTS +/- DC LEVEL
58                  ;       1       1       NO CHANGE IN DC LEVEL DURING Z PULSE
```

```
|0006 .MAIN
01                  ;       ALL PROGRAMMED I/O DIGITAL-TO-ANALOG CONVERSIONS
02                  ;       SHOULD NORMALLY BEGIN WITH A DOCS INSTRUCTION. THE
03                  ;       DOC INSTRUCTION WILL LOAD THE FIRST BUFFER WITH DATA.
04                  ;       PIO CONVERSIONS THAT ARE SYNCHRONIZED TO AN INTERNAL
05                  ;       OR EXTERNAL CLOCK WILL OCCUR WITHOUT THE START COMMAND,
06                  ;       ON THE FIRST FALLING EDGE OF THE CLOCK PULSE AFTER
07                  ;       THE DOC COMMAND HAS BEEN ISSUED. HENCE, IF IT IS
08                  ;       DESIRED TO DO PROGRAMMED, SYNCHRONIZED CONVERSIONS
09                  ;       WITHOUT SETTING CONE, THE DOC COMMAND ALONE MAY BE
10                  ;       GIVEN. FOR NON-SYNCHRONIZED PROGRAMMED I/O CONVERSIONS,
11                  ;       THE I/O START COMMAND MUST BE GIVEN TO SEND THE DATA
12                  ;       FROM THE FIRST BUFFER TO THE SECOND BUFFER AND OUT
13                  ;       TO THE DACS FOR CONVERSION.
14
15                  ;       FOR DATA CHANNEL TRANSFERS, THE I/O START COMMAND CAUSES
16                  ;       THE FIRST DATA CHANNEL TRANSFER TO THE FIRST BUFFER.
17                  ;       SUBSEQUENTLY, THE CLOCK SOURCE SELECTED BY THE
18                  ;       DOA INSTRUCTION OUTPUTS THE DATA TO THE APPROPRIATE
19                  ;       DAC AND REQUESTS ANOTHER DATA CHANNEL TRANSFER.
20
21                  ;       THE EVENT WHICH CAUSES DONE TO BE SET VARIES, DEPENDING
22                  ;       ON THE MODE IN WHICH INTERFACE IS BEING USED. FOR
23                  ;       UNSYNCHRONIZED CONVERSIONS IN WHICH THE SCOPE MODE IS
24                  ;       NOT BEING USED (NO Z-AXIS PULSES TRIGGERED AFTER THE
25                  ;       CONVERSION), THE DOCS COMMAND TO START A CONVERSION
26                  ;       WILL, OF COURSE, SET BUSY BUT DONE WILL NEVER BE SET
27                  ;       IN THIS MODE BECAUSE OF THE FAST SPEED OF THE CON-
28                  ;       VERSION (BUSY WILL REMAIN SET). BEFORE NEW STATUS BITS
29                  ;       ARE SELECTED (VIA A DOA INSTRUCTION), BUSY SHOULD BE
30                  ;       CLEARED (VIA AN I/O CLEAR). DONE IS SET AS FOLLOWS:
31
```

```
;       DOA INSTRUCTION STATUS BITS     DONE SETTING SOURCE
;       ===========================     ===================
;       MODE    CLOCK   /SCOPE
;       DCH     SYNC    MODE/
;       ==      ==      ==
;       D0      D1      C4
;       ==      ==      ==

;       0       0       0               END OF Z PULSE

;       0       0       1               NONE

;       0       1       0               END OF Z PULSE

;       0       1       1               2ND BUFFER CLOCK PULSE
;                                       (FALLING EDGE OF
;                                       EXTERNAL/INTERNAL CLK
;                                       INDICATES DATA SENT
;                                       TO DAC)

;       1       0       0               END OF Z PULSE AFTER
;                                       /WCEZ/ (NOTE: LAST
;                                       DATA CHANNEL WORD MUST
;                                       CAUSE Z PULSE OR ELSE
;                                       DONE WILL NOT SET)

;       1       0       1               2ND BUFFER CLOCK PULSE
;                                       AFTER /WCEZ/(SYCHRONIZED
;                                       TO FALLING EDGE OF
;                                       /IOPLS/ OR /DATA READY/
;                                       = INDICATES LAST DATA
;                                       IN DCH TRANSFER HAS
;                                       BEEN SENT TO DAC

;       1       1       0               END OF Z PULSE AFTER
;                                       /WCEZ/ (SEE NOTE ABOVE)

;       1       1       1               2ND BUFFER CLOCK PULSE
;                                       AFTER /WCEZ/, SYNCHRO=
;                                       NIZED TO FALLING EDGE
;                                       OF INTERNAL/EXTERNAL
;                                       CLOCK = INDICATES LAST
;                                       DATA IN DCH TRANSFER HAS
;                                       BEEN SENT TO DAC

;       NOTE = IN THE DATA CHANNEL MODES ABOVE, DONE MAY
;       ALSO BE SET BY THE LATE CONVERSION SIGNAL, IF THE
;       APPROPRIATE JUMPER CONNECTION IS MADE.
```



```
;       IF THE PERIOD OF THE SYNCHRONIZING CLOCK IN DATA
;       CHANNEL MODE IS LESS THAN THE DATA CHANNEL LATENCY
;       TIME, DATA WILL NOT BE LOST, BUT IT WILL NOT APPEAR
;       AT THE DAC AT THE CORRECT SYNCHRONIZING CLOCK EDGE.
;       RATHER, IT WILL APPEAR AT THE APPROPRIATE DAC AT THE
;       TIME OF THE FIRST TRAILING EDGE OF THE CLOCK AFTER
;       THE FIRST BUFFER HAS BEEN LOADED WITH NEW DATA. THE
;       DATA APPEARING AT THE DACS IS LATE FOR SYN=
;       CHRONIZATION, HOWEVER, AND THE LATE CONVERSION SIGNAL
;       IS SET. THIS SIGNAL MAY BE READ IN AS A STATUS
;       BIT BY A DIA INSTRUCTION AND MAY, BY
;       SETTING A JUMPER, SET DONE. THE LATE CONVERSION
;       SIGNAL IS CLEARED BY AN I/O CLEAR OR DOA INSTRUCTION.

;       IF THIS INTERFACE IS BEING USED TO DISPLAY ON A SCOPE
;       AN ARRAY OF POINTS LOCATED IN MEMORY, DATA CHANNEL
;       MODE SHOULD BE USED WITH THE ALTERNATE BIT SET, THE
;       /SCOPE MODE/ BIT RESET (THIS IS AN ACTIVE=LOW SIGNAL)
;       AND DATA ARRAYED IN MEMORY XYXYXYXY...OR YXYXYXYX...
;       IN THE FORMER CASE, DAC X IS SELECTED AS THE FIRST
;       DAC TO RECEIVE DATA AND THE SCOPE CIRCUITRY IS JUMPED
;       SO THAT A Z PULSE OCCURS AFTER CLOCK Y, AND THE
;       BRIGHTNESS CIRCUIT IS JUMPERED FOR BRTYMSB AND
;       BRTYLSB. FOR THE YXYXYXYX... ORIENTATION, SET UP
;       IS REVERSED. THE Z DELAY (7 US) + THE Z PULSE
;       WIDTH MAY NOT EXCEED THE CLOCK PERIOD. HENCE,
;       THE Z INTENSIFICATION PULSE IS DONE BEFORE ANY DAC IS
;       UPDATED WITH NEW DATA.

;       AN EXTERNAL INTERRUPT MAY BE REQUESTED BY PULLING THE
;       /EXTERNAL INTERRUPT/ LINE LOW, WHICH WILL REQUEST AN
;       INTERRUPT WITHOUT SETTING DONE. THE EXTERNAL
;       INTERRUPT REQUEST IS CLEARED BY AN I/O CLEAR OR DOA
;       INSTRUCTION.

;       A DIA INSTRUCTION INPUTS FOUR STATUS BITS TO THE CPU:
;       AN EXTERNAL ERASE INPUT BIT WHICH IS SET BY PULLING
;       THE /EXTERNAL ERASE INPUT/ LINE LOW; A DATA READY BIT
;       TO INDICATE THAT NEW DATA HAS BEEN LOADED INTO THE
;       FIRST BUFFER (USEFUL FOR THE IOPLS DATA CHANNEL MODE)
;       A LATE CONVERSION ERROR BIT; AND A BIT INDICATING
;       THE PRESENCE OF AN EXTERNAL INTERRUPT.

;       THE FOLLOWING ARE THE NOMINAL RANGES (PERIODS) FOR
;       THE INTERNAL CLOCK AND THE ZPULSE (ADJUSTABLE BY
;       POTENTIOMETERS ON THE D/A BOARD):

;       WHAT            MIN     MAX     POT.
;       ====            ===     ===     ====
;       INTERNAL CLOCK  16 US   190 US  R43
;       ZPULSE          4 US    150 US  R32
```

```
;7.2:   PROGRAM OPERATION:
;       THIS DIAGNOSTIC IS INTENDED TO TEST THE FOLLOWING
;       LOGIC AND/OR FUNCTIONS: BUSY, DONE, START, CLEAR
;       IORST (DAC RST), IOPLS, D/A MODE REGISTER (DOA),
;       DCH ADDRESS REGISTER (DOB/DIB), DCH WORD COUNT
;       (DOC), DAC LOAD (DOC IN PIO MODE), D/A STATUS
;       REGISTER (DIA), INTERRUPT REQUESTS, INTERRUPT
;       DISABLE (MSKO), D/A CONVERSIONS (PIO/START,
;       PIO/INTERNAL CLOCK, DCH/IOPLS, DCH/DATA READY,
;       DCH/INTERNAL CLOCK), DCH RANDOM ADDRESS EXERCISER
;       DAC SELECT, Z-AXIS PULSE TRIGGERING (ZPULSE),
;       SCOPE MODE, ALTERNATE, DATA READY, LATE CONVERSION
;       (WILL CHECK IF ANY OCCUR) AND MISC TESTS.
;       OPTIONAL TESTS ARE INCLUDED TO TEST: EXTERNAL
;       CLOCK OPERATION (PIO/DCH), EXTERNAL INTERRUPT
;       REQUESTS AND EXTERNAL ERASE INPUT.

;       THE PROGRAM CHECKS THE ABOVE THROUGH A SERIES
;       OF SUBTESTS. IF NO ERROR IS FOUND, THE PROGRAM
;       WILL PERFORM THE TESTS IN SEQUENCE UNTIL THE LAST
;       TEST, AT WHICH TIME AN END OF PASS MESSAGE WILL
;       BE PRINTED. IF AN ERROR OCCURS, THE OPERATOR WILL BE
;       INFORMED OF IT. TO FIND THE PROBLEM, REFER TO THE
;       ASSOCIATED ERROR NUMBER AND PROGRAM COUNTER IN
;       THE DIAGNOSTIC LISTING. TO FIND THE ACTUAL HARDWARE
;       FAILURE, SET UP A SCOPE LOOP (SEE SECTION 8)
;       AND TRACE THE FAILURE WITH AN OSCILLOSCOPE.
;       THE COMMENTS IN THE LISTING WILL GIVE THE OPERATOR
;       INFORMATION ABOUT THE PROBLEM AS WELL AS
;       INFORMATION CONCERNING THE ACCUMULATOR CONTENTS.
;       AFTER ALL SUBTESTS (ONE PASS) HAVE BEEN PERFORMED
;       THE DIAGNOSTIC WILL REPEAT THE TEST SEQUENCE STARTING
;       WITH THE FIRST SUBTEST.
```



```
;8.      OPERATING MODES/SWITCH COMMANDS:
;        ================================
;        LOCATION "SWREG" IS USED TO SELECT THE PROGRAM OPTIONS
;        (NOT SYSTEM CONFIGURATION). WHILE RUNNING UNDER DTOS,
;        THIS LOCATION WILL BE LOADED BY THE MONITOR.
;        HOWEVER UNDER STAND ALONE AND PROGRAM LOAD MODES THIS
;        LOCATION WILL BE SET ACCORDING TO THE ANSWERS SUPPLIED
;        BY THE OPERATOR. IN ANY CASE THE OPTIONS CAN BE CHANGED
;        OR VERIFIED BY USING ONE OF THE COMMANDS GIVEN IN SEC.
;        8.2

;8.1     SWITCH OPTIONS
;        DIFFERENT BITS AND THEIR INTERPRETATION AT LOCATION
;        "SWREG" IS AS FOLLOWS:

;        BIT     OCTAL   BINARY  INERPRETATION
;                VALUE   VALUE

;        1               0       LOOP ON ERROR
;                40000   1       SKIP LOOPING ON ERROR

;        2               0       PRINT TO CONSOLE
;                20000   1       ABORT PRINT OUT TO CONSOLE

;        3               0       DO NOT PRINT % FAILURE
;                10000   1       PRINT % FAILURE

;        4               0       ALLOW END OF PASS PRINT OUT
;                04000   1       SUPPRESS END OF PASS PRINT OUT

;        5               0       DO NOT PRINT ON THE LINE PRINTER
;                02000   1       PRINT ON THE LINE PRINTER

;        6               0       DO NOT HALT ON ERROR
;                01000   1       HALT ON ERROR

;        7               0       DO NOT PRINT SUMMARY AND/OR
;                                PASSING OF EACH SUBTEST
;                00400   1       PRINT SUMMARY AND/OR
;                                PASSING OF EACH SUBTEST

;        8               0       PRINT ONLY THE FIRST ERROR
;                00200   1       PRINT EVERY ERROR
```

```
;8.2     SWITCH COMMANDS
;        ONCE THE PROGRAM STARTS EXECUTING THE STATE OF ANY OF
;        THE BITS CAN BE CHANGED BY HITTING KEYS 1-9, A-F. THE
;        PROGRAM WILL CONTINUE RUNNING AFTER UPDATING THE OPTIONS
;        EACH KEY WILL COMPLEMENT THE STATE OF THE BIT AFFILIAT-
;        ED WITH IT, THUS BIT 4 CAN BE ALTERED BY HITTING KEY 4.
;        SETTING OF ANY BIT OF LOCATION "SWREG" WILL SET BIT 0.
;        (DEFAULT MODE IS DEFINED AS ALL BITS OF SWREG SET TO 0)
;        THE PROGRAM CAN BE LOCKED INTO SWITCH MODIFICATION MODE
;        BY TYPING A 0, IN WHICH CASE MORE THAN ONE BIT CAN BE
;        CHANGED BEFORE  CONTROL IS ALLOWED TO RETURN TO THE
;        MAIN PROGRAM.
;
;8.2.1   OTHER COMMANDS
;        "CR"     A "RETURN" CAN BE TYPED TO CONTINUE THE PROGRAM
;                 AFTER ITS LOCKED IN A SWITCH MODIFICATION MODE
;
;        ^D       THIS COMMAND GIVEN AT ANY TIME WILL RESET "SWREG
;                 TO DEFAULT MODE AND RESTART THE PROGRAM.
;
;        ^R       THIS COMMAND GIVEN AT ANY TIME WILL RESTART THE
;                 PROGRAM. SWITCHES ARE LEFT WITH THE VALUES THEY
;                 HAD BEFORE THE COMMAND WAS ISSUED.
;
;        ^O       THIS COMMAND GIVEN AT ANY TIME WILL CAUSE THE
;                 PROGRAM CONTROL TO GO TO ODT (NOTE: THIS IS AN
;                 OPTIONAL COMMAND AND IS AVAILBLE ONLY IF
;                 ODTPK IS PRESENT)
;
;        M        THIS COMMAND GIVEN AT ANY TIME WILL PRINT THE
;                 CURRENT OPERATING MODES.
```



```
;8.3     SELECTION OF SPECIAL TEST FUNCTIONS:
;        THE FOLLOWING "SWREG" SWITCHES CONTROL THE OPERATION
;        OF CERTAIN OPTIONAL TESTS. FOR ALL OF THE FOLLOWING:

;        SWITCH = 0       TEST IS SKIPPED
;        SWITCH = 1       TEST IS PERFORMED

;        SWITCH           TEST
;        C                EXTERNAL CLOCK TEST
;        D                EXTERNAL INTERRUPT TEST
;        E                EXTERNAL ERASE INPUT TEST

;        NOTE THAT IF THESE FUNCTIONS DO NOT OPEARTE BECAUSE
;        OF A HARDWARE ERROR, IT IS POSSIBLE FOR THE DIAGNOSTIC
;        TO REMAIN IN THE TEST LOOP. HOWEVER, FOR ANY OF THE
;        ABOVE TESTS SELECTED, THE PROGRAM WILL PRINT A MESSAGE
;        TO THE OPERATOR INDICATING WHICH TEST IS BEING
;        PERFORMED (AND INDICATING OPERATOR ACTION). IF THE
;        FUNCTION IS OPERATING PROPERLY, A "COMPLETED SUBTEST"
;        MESSAGE WILL BE PRINTED. THE ABSENCE OF THIS MESSAGE
;        AFTER THE OPERATOR HAS PERFORMED THE OPERATION
;        INDICATES A HARDWARE FAILURE. IN THIS CASE THE ERROR
;        CAN BE FOUND BY USING AN OSCILLOSCOPE FOR ERROR
;        TRACING, AS THE DIAGNOSTIC IS IN A SCOPE LOOP.

;        THE FOLLOWING OPERATOR ACTIONS ARE EXPECTED FOR
;        THE ABOVE TESTS (IF SELECTED):

;        TEST             ACTION EXPECTED
;        EXT CLK          PULSE THE EXTERNAL CLOCK LINE (A1)
;                         AT LEAST (4) TIMES (A PULSE GENERATOR
;                         CAN BE USED FOR THIS)
;                         EXTERNAL CLOCK IS HIGH ACTIVE.
;        EXT INTERRUPT    GROUND THE EXTERNAL INTERRUPT
;                         REQUEST LINE (A3) ONCE (LOW ACTIVE).
;        EXT ERASE IN     GROUND THE EXTERNAL ERASE INPUT
;                         LINE (A15) ONCE (LOW ACTIVE).

;        NOTE: EXTERNAL CLOCK CAN BE SELF-TESTED BY CONNECTING
;        THE INTERNAL CLOCK OUTPUT (A17) TO THE EXTERNAL CLOCK
;        INPUT (A1) AND SELECTING THE OPTIONAL EXTERNAL CLOCK
;        TEST (SEE ABOVE).
```

```
;8.4     SETTING UP A SCOPE LOOP:

;        THIS DIAGNOSTIC CAN BE USED TO TRACE FAILURES ON
;        DETECTION OF AN ERROR. IF, AND WHEN AN ERROR IS
;        DETECTED DURING TESTING, A DIAGNOSTIC SCOPE LOOP CAN
;        BE FORMED BY DOING THE FOLLOWING:

;        1) "SWREG" SWITCH 1 MUST BE EQUAL = 0 (LOOP ON ERROR).
;        2) NOTE THE PROGRAM COUNTER (PC) CONTENTS, THE SUB-
;           TEST #, THE ERROR # AND THE ACCUMULATOR CONTENTS.
;        3) SUPRESS ALL TTY/LPT OUTPUTS BY SETTING SWITCH 2 = 1
;           AND SWITCH 5 = 0.
;        4) GO TO THE FAILING ADDRESS (= PROGRAM COUNTER) IN THE
;           DIAGNOSTIC LISTING FOR THE INSTRUCTION SEQUENCE (AND
;           INFORMATION) THAT CAUSED OR DETECTED THE ERROR.
;        5) IF THE SCOPE LOOP CONTAINS AN I/O RESET (MNRST) IN IT
;           THE SCOPE LOOP FORMED WILL BE SLOW. IT CAN BE SPEEDED
;           UP BY FOLLOWING THE INSTRUCTIONS IN SECTION 11.7.
;        6) THE SCOPE LOOP SHOULD NOW BE READY TO USE. (HELPFUL
;           ITEMS ARE AN OSCILLOSCOPE, SCHEMATICS, PHYSICAL).
```



```
;9.      OPERATING PROCEDURE/OPERATOR INPUT
;        ==================================
;        NOTE: POWER SHOULD ALWAYS BE OFF DURING INSERTION
;        AND REMOVAL OF THE D/A INTERFACE (OR ANY BOARD)
;        INTO MICRO NOVA CHASSIS.

;        TO RUN THIS DIAGNOSTIC:

;        1.  INSERT D/A INTERFACE INTO AN I/O SLOT
;            WITH THE INTERRUPT PRIORITY (/INTP/) AND
;            DATA CHANNEL PRIORITY (/DCHP/) I/O LINES
;            PROPERLY JUMPERED.
;        2.  LOAD THE DIAGNOSTIC VIA PAPER TAPE OR
;            DOOS DISKETTE.
;        3.  STARTING ADDRESS IS 200 (OR 500) OCTAL
;        4.  AFTER THE PROGRAM HAS BEEN STARTED, THE
;            MEMORY WILL BE SIZED AND THE MESSAGE

;            "TOP OF MEMORY = XXXXXX"

;            WILL BE PRINTED WHERE XXXXXX IS THE
;            HIGHEST LOGICAL MEMORY ADDRESS IN
;            OCTAL.
;        5.  ANSWER THE FOLLOWING QUESTIONS:

;            "DEVICE CODE = "

;            ENTER THE 6-BIT DEVICE CODE OF THE
;            DIA INTERFACE IN OCTAL.
;            (MUST BE < 77 OCTAL).

;            "Z-AXIS PULSE TRIGGERED BY:(0=CLOCK X, 1=CLOCK Y)="

;            THIS REFERS TO THE Z-AXIS CLOCK TRIGGERING JUMPER
;            ON THE D/A. BOARD (SEE SECTION 4).

;        THE DIAGNOSTIC WILL THEN BEGIN OPERATION ACCORDING TO
;        THE MODES SELECTED BY "SWREG" (SEE SECTION 6).
;        IF AN INCORRECT RESPONSE IS MADE TO ANY QUESTION
;        IT WILL BE RE-TYPED.
```

```
;10.    PROGRAM OUTPUT/ERROR DESCRIPTION:
;       ================================
;       ALL PROGRAM OUTPUTS, BOTH MESSAGES AND ERROR
;       REPORTS, ARE CONTROLLED BY THE VALUE OF "SWREG"
;       (SEE SECTION 8) SWITCHES 2 AND 5 AS FOLLOWS:

;       SWITCH          PRINTOUT TO
;       2    5          TTY/CRT  LPT
;       =====           ==========
;       0    0          YES      NO
;       0    1          YES      YES
;       1    0          NO       NO
;       1    1          NO       YES

;       IF AN ERROR IS ENCOUNTERED DURING DIAGNOSTIC
;       OPERATION, THE PROGRAM WILL PRINT OUT THE
;       FOLLOWING ERROR REPORT:

;       ERROR NUMBER #  ENCOUNTERED SUBTEST #
;       CRY     AC0     AC1     AC2     AC3     PC
;       X       XXXXXX  XXXXXX  XXXXXX  XXXXXX  XXXXXX

;       WHERE:  CRY = CARRY
;               PC = PROGRAM COUNTER (FAILING ADDRESS)
;               AC0, AC1, AC2, AC3 = ACCUMULATOR CONTENTS
;               (CONTENTS DEPEND ON SPECIFIC TEST)

;       ALL NUMERIC VALUES ARE IN OCTAL. THE ACTION
;       TAKEN AFTER ERROR MESSAGE PRINTOUT DEPENDS ON
;       THE VALUE OF "SWREG" (SEE SECTION 8). IF SWITCH
;       6 = 1 THEN THE PROGRAM WILL HALT AFTER THE
;       MESSAGE "HALTED ON ERROR" IS PRINTED. IF SWITCH
;       1 = 0 THEN THE PROGRAM WILL LOOP ON THE ERROR
;       AFTER THE MESSAGE "LOOPING ON ERROR" IS PRINTED.
;       THIS FORMS A TEST SCOPE LOOP FOR FAILURE TRACING
;       WITH AN OSCILLOSCOPE. IF SWITCH 1 = 0 AND SWITCH 6 = 1
;       THE PROGRAM WILL FIRST HALT, THEN LOOP ON THE
;       ERROR IF THE PROGRAM IS CONTINUED. IF SWITCH 8
;       = 1 THEN ONLY THE FIRST ERROR WILL BE REPORTED.
;       IF THE PROGRAM IS LOOPING ON AN ERROR AND "SWREG"
;       SWITCH 3 = 1, A SUBTEST FAILURE RATE IS REPORTED
;       AS "SUBTEST (#)  FAILED (X) %", WHERE (#) IS THE
;       LOOP TEST NUMBER IN OCTAL AND (X) IS A DECIMAL %.
;       (NOTE: WHEN LOOPING ON A TEST THAT HAS MORE THAN
;       ONE ERROR BEING DETECTED, AND A % FAILURE RATE IS
;       BEING REPORTED, THE FAILURE RATE WILL APPEAR AS
;       X00% WHERE X IS THE # OF ERRORS OCCURING. FOR
;       EXAMPLE, A SCOPE LOOP WITH 2 ERRORS WOULD REPORT
;       "SUBTEST (#) FAILED 200%".)

;       AFTER ALL SUBTESTS HAVE BEEN PERFORMED (ONE PASS)
;       THE PROGRAM WILL REPORT "END OF PASS" (#). (#)
;       IS AN OCTAL VALUE.
```



```
;       IF SWITCH 7 = 1, THE PROGRAM WILL INFORM THE
;       OPERATOR WHEN A SUBTEST HAS BEEN COMPLETED BY
;       PRINTING "COMPLETED SUBTEST (#)", WHERE (#) IS
;       THE SUBTEST NUMBER IN OCTAL. IN ADDITION, WHEN
;       SWITCH 7 GOES FROM 0 TO 1, AN ERROR SUMMARY WILL
;       BE PRINTED AS FOLLOWS:

;       ERROR SUMMARY REPORT FOLLOWS
;       ERROR NUMBER: (#1)  (#2) ... (#N)
;       END OF SUMMARY

;       WHERE (#1)  (#2) ... (#N) IS A LIST OF ALL ERROR
;             NUMBERS THAT HAVE BEEN DETECTED. IF NO
;             ERRORS HAVE OCCURED, THEN THE MESSAGE
;             "NO ERRORS ENCOUNTERED SINCE LAST SUMMARY"
;             WILL BE REPORTED INSTEAD.

;       OTHER ERRORS:

;       1.  "FATAL SUBTEST SEQUENCE ERROR ENCOUNTERED"
;           IS REPORTED, FOLLOWED BY A HALT, IF ANY
;           TEST IS PERFORMED OUT OF SEQUENCE (I.E.
;           1, 2, 3, 5 INSTEAD OF 1, 2, 3, 4). NO
;           SEQUENCE CHECK IS MADE FOR ANY SELECTED
;           OPTIONAL TESTS (SEE SECTION 8.3).

;       2.  "FATAL STACK BOUNDARY VIOLATION. SP = (XXXXXX)"
;           IS REPORTED, FOLLOWED BY A HALT, IF A
;           STACK BOUNDARY IS CROSSED (256 WDS). XXXXXX
;           IS THE VALUE OF THE STACK POINTER (OCTAL).

;       3.  "*** RTC FAILURE ****" IS REPORTED, FOLLOWED
;           BY A HALT IF THE REAL-TIME CLOCK FAILS TO
;           CAUSE INTERRUPTS DURING TIMER VALUE CALCULATIONS.

;       4.  "UNIDENTIFIED INTERRUPT = (DVC)"
;           FOLLOWED BY AN ERROR PRINTOUT (SEE ABOVE) IS
;           REPORTED IF ANY DEVICE OTHER THAN THE D/A
;           INTERFACE REQUESTS AN INTERRUPT DURING DIAG-
;           NOSTIC OPERATION. DVC = THE OCTAL DEVICE CODE
;           OF THE DEVICE REQUESTING THE INTERRUPT. ALSO,
;           THE PROGRAM WILL ATTEMPT TO CLEAR THE INTERRUPT
;           BY ISSUING AN 'NIOC' INSTRUCTION TO THE DEVICE.

;       5.  "EXTERNAL INTERRUPT = (DVC)"
;           FOLLOWED BY AN ERROR PRINTOUT (SEE ABOVE) IS
;           REPORTED IF AN UNEXPECTED D/A EXTERNAL INTERRUPT
;           (CAUSED BY GROUNDING THE /EXT INT REQ/ LINE)
;           DURING DIAGNOSTIC OPERATION. THE INTERRUPT
;           IS NOT CLEARED BY THE INTERRUPT SERVICE ROUTINE.
;           HOWEVER, IF THE EXTERNAL INTERRUPT OCCURS
;           DURING THE EXTERNAL INTERRUPT TEST (SEE 8.3)
;           THE MESSAGE WILL BE PRINTED, INDICATING THAT
;           ONE WAS RECEIVED, BUT NO ERROR MESSAGE WILL
;           FOLLOW. DVC IS THE D/A DEVICE CODE (OCTAL).
```

```
;11.     DEBUG HELP:
;        ----------
;        *** OCTAL DEBUG TOOL (ODT) ***
;
;        THE DIAGNOSTIC IS EQUIPED WITH A BUILT IN ODT WHICH CAN
;        BE ACCESSED BY HITTING CONTROL O (↑O) AT ANY TIME DURING
;        THE EXECUTION OF THE PROGRAM (AFTER SETTING THE PARA-
;        METERS).
;        ON ENTERING ODT THE ADDRESS OF THE LOCATION HAVING THE
;        NEXT INSTRUCTION TO BE EXECUTED WILL BE TYPED-OUT.
;
;11.1    CONVENTIONS AND SYMBOLS
;        THE FOLLOWING CONVENTIONS ARE USED BY THE ODT:
;        ?        PRESSING ANY ILLEGAL KEY CAUSES THE ODT TO RES-
;                 POND WITH A "?".
;        @        ODT IS READY AND AT YOUR SERVICE.
;
;11.2    COMMAND STRUCTURE
;        AN ODT COMMAND HAS THE FOLLOWING FORMAT:
;                 [ARGUMENT][COMMAND]
;        AN ARGUMENT MAY BE ONE OF THE FOLLOWING:
;        "EXP"    AN OCTAL EXPRESSION CONSISTING OF OCTAL NUMBERS
;                 SEPARATED BY PLUS (+) OR MINUS (-) SIGNS. LEAD-
;                 ING ZEROS NEED NOT BE TYPED.
;        "ADR"    AN ADDRESS IS THE SAME AS AN EXPRESSION EXCEPT
;                 THAT BIT 0 IS NEGLECTED.
;        A COMMAND IS A SINGLE TELETYPE CHARACTER
;
;11.3    ODT COMMANDS
;        THE LOCATIONS THAT CAN BE EXAMINED AND MODIFIED BY THE
;        USER ARE CALLED CELLS. THESE CELLS ARE OF TWO TYPES:
;        INTERNAL CPU CELLS AND MEMORY LOCATIONS.
;
;11.3.1 OPENING INTERNAL CELLS
;        THE COMMAND TO OPEN ONE OF THE INTERNAL REGISTERS IS OF
;        THE FORM "NA" WHERE N IS ANY OCTAL EXPRESSION BETWEEN
;        0 AND 7
;        0-3      FOR ACCUMULATORS 0-3
;        4        FOR PC OF THE NEXT INSTRUCTION TO BE EXECUTED IN
;                 THE EVENT OF A "P" COMMAND.
;        5        CPU AND TTO STATUS
;                 BIT      INTERPRETATION
;                 15       STATUS OF TTO DONE FLAG
;                 14       STATUS OF INTERRUPTS (ION FLAG)
;                 13       STATUS OF CARRY BIT
;        6        ADDRESS OF THE LOCATION HAVING THE BREAK POINT (
;                 ANY)
;        7        INSTRUCTION AT THE BREAK POINT LOCATION
```



```
;        OTHER COMMANDS TO OPEN CELLS ARE:
;
;        "ADR"/  OPEN THE CELL AND PRINT ITS CONTENTS
;        ./      OPEN THE CELL CURRENTLY POINTED TO BY THE POINTE
;                AND PRINT ITS CONTENTS.
;        .+"ADR"/         ADD "ADR" TO THE POINTER, OPEN THE CELL
;                ITS CONTENTS.
;        .-"ADR"/         SUBTRACT "ADR" FROM THE POINTER, OPEN TH
;                PRINT ITS CONTENTS.
;        "CR"    THE RETURN KEY IS USED TO CLOSE THE OPEN CELL
;                WITH OR WITHOUT MODIFICATION.
;        "LF"    LINE FEED IS USED TO CLOSE THE OPEN CELL WITH OR
;                WITHOUT MODIFICATION AND TO OPEN THE SUCCEEDING
;                CELL.
;        ↑       CLOSE THE OPEN CELL WITH OR WITHOUT MODIFICATION
;                AND OPEN THE PRECEDING CELL
;        /       CLOSE THE OPEN CELL WITHOUT MODIFICATION, AND
;                OPEN THE CELL POINTED TO BY ITS CONTENTS.
;        +"ADR"/ CLOSE THE OPEN CELL WITHOUT MODIFICATION, AND
;                OPEN THE CELL POINTED TO BY ITS CONTENTS + "ADDR
;        -"ADR"/ CLOSE THE OPEN CELL WITHOUT MODIFICATION, AND
;                OPEN THE CELL POINTED TO BY ITS CONTENTS - "ADR"
;
;11.3.2 MODIFICATION OF A CELL
;        ONCE A CELL HAS BEEN OPENED ITS CONTENTS CAN BE MODIFIED
;        BY TYPING THE NEW VALUE THE CELL IS TO CONTAIN IN THE
;        FORM OF AN OCTAL EXPRESSION FOLLOWED BY "CR" OR "LF".
;        IF A + OR - IS TYPED AS THE FIRST CHARACTER OF THE EX-
;        PRESSION THEN THE VALUE OF THE EXPRESSION IS ADDED TO OR
;        SUBTRACTED FROM THE OLD CONTENTS OF THE CELL. THE
;        ADDRESS ITSELF OR AN EXPRESION RELATIVE TO THE ADDRESS
;        CAN BE DEPOSITED BY TYPING A "." OR ".+/-OCTAL EXPRESS-
;        ION". A RUBOUT COMMAND GIVEN RIGHT AFTER OPENING A CELL
;        ALLOWS THE MODIFICATION OF ITS CONTENTS AS IF THEY WERE
;        TYPED IN JUST BEFORE THE COMMAND WAS ISSUED.
;
```

```
;11.3.3 OTHER ODT COMMANDS
;       RUBOUT   THIS KEY IS USED TO DELETE ERRONEOUSLY TYPED
;                DIGITS. EACH TIME THE KEY IS PRESSED THE RIGHT M
;                DIGIT IS DELETED AND ECHOED ON THE TERMINAL. IF
;                THE RUBOUT KEY IS PRESSED RIGHT AFTER OPENING A
;                CELL THEN IT DELETES THE RIGHT MOST DIGIT OF THE
;                CONTENTS. THIS ALLOWS THE MODIFICATION OF THE CE
;                AS IF ITS CONTENTS WERE TYPED IN JUST BEFORE THE
;                KEY WAS PRESSED.
;       "ADR"B   INSERT A BREAK POINT AT LOCATION "ADR".
;                ONLY ONE BREAK POINT CAN BE INSERTED AND ANY
;                ENTRY TO ODT AFTER EXECUTING A BREAK POINT WILL
;                CAUSE IT TO BE DELETED.
;       D        DELETE THE BREAK POINT IF ANY.
;       P        RESTART THE EXECUTION OF THE PROGRAM AT LOCATION
;                POINTED BY 4A.
;       "ADR"R   START EXECUTING THE PROGRAM AT "ADR" AFTER AN
;                IO-RESET.
;       K        KILL THE STRING TYPED SO FAR. THE ODT RESPONDS
;                WITH A "?" AND THE OPEN CELL IS CLOSED WITHOUT
;                MODIFICATION.
;       =        PRINT THE OCTAL VALUE OF THE INPUT ONLY.
;                THIS WILL CLOSE ANY OPEN CELLS WITHOUT
;                MODIFICATION AND WILL NOT OPEN A CELL
;
;
;       NOTE:    IN PROGRAMS WHICH RELOCATE THEMSELVES THE
;                THE USER SHOULD PLACE BREAK POINTS ONLY IN THE
;                THE ORIGINAL PROGRAM AREA. IF A BREAK POINT IS
;                PLACED OUTSIDE THIS AREA THE RESULTS WILL
;                BE UNPREDICTABLE.
```



```
;11.4   INSTRUCTION SET:
;       DOA:  OUTPUT STATUS BITS TO THE INTERFACE, CLEARS
;       EXTERNAL INTERRUPT REQUEST AND LATE CONVERSION.
;       SHOULD NOT BE GIVEN IF BUSY IS SET AND MUST APPEAR
;       BEFORE DOB AND DOC IN DATA CHANNEL SETUP SEQUENCE.

;       D0, D1, D2 ARE THE CLOCK SOURCE BITS FOR SENDING
;       DIGITAL DATA TO THE D/A CONVERTERS:

;       D0      D1      D2      CLOCK SOURCE TO SEND DAC DATA
;       --      --      --      ----------------------------
;       0       0       0       /STRT/, NO SYNC
;       0       0       1       NO CONVERSIONS
;       0       1       0       INTERNAL CLOCK SYNC *
;       0       1       1       EXTERNAL CLOCK SYNC *
;       1       0       0       /IOPLS/ (1 DATA CONVERSION
;                               FOR EVERY /IOPLS/ FOLLOWING
;                               /STRT/, NO SYNC) **
;       1       0       1       /DATA READY/ (OCCURS 1
;                               FSTROBE CYCLE AFTER /DCHO/
;                               & IS MAXIMUM TRANSFER RATE)
;       1       1       0       INTERNAL CLOCK SYNC
;       1       1       1       EXTERNAL CLOCK SYNC

;       * FIRST FALLING EDGE AFTER DOC COMMAND
;       ** DATA SHOULD BE READY IN THE FIRST BUFFER BEFORE
;          /IOPLS/ IS ISSUED

;D3     ALTERNATE BIT     0     DO NOT ALTERNATE BETWEEN
;                               DAC X AND DAC Y.

;                         1     ALTERNATE BETWEEN DAC X AND
;                               DAC Y, STARTING WITH DAC
;                               SELECTED BY D15

;D4     /SCOPE MODE/ BIT  0     Z-AXIS PULSE GIVEN EVERY TIME
;                               DAC X OR DAC Y (JUMPER
;                               SELECTABLE) IS WRITTEN TO


;                         1     NO Z-AXIS PULSES OUTPUTTED

;D5     /NON-STORE/       1     FOR NON-STORE, OC TRUE-LOW
;                               OUTPUT (PINS A9 AND A10)

;D6     /WRITE-THROUGH/   1     FOR WRITE-THROUGH, OC TRUE-LOW
;                               OUTPUT (PINS A11 AND A12)

;D7     /ERASE/           1     FOR 2 MS PULSE TO SCOPE,
;                               OC TRUE-LOW OUTPUT
;                               (PINS A13 AND A14)

;D15    DAC SELECT BIT    0     SELECTS DAC X
;                         1     SELECTS DAC Y

;       THE DEFAULT STATE OF ALL THESE STATUS BITS
;       UPON POWER-UP OR IORST IS 0.
```

```
;DOB:   OUTPUTS TO ADDRESS REGISTER FOR DATA CHANNEL
;       TRANSFERS.

;DOC:   OUTPUTS TO WORD-COUNT REGISTER FOR DATA CHANNEL
;       TRANSFERS. IN PROGRAMMED I/O MODE (DB=0 IN
;       DOA INSTRUCTION) THIS INSTRUCTION CAUSES THE
;       FIRST BUFFER TO BE LOADED WITH THE DATA IN
;       THE ACCUMULATOR BITS 0-11, 14 AND 15.
;       BITS 0-11 ARE THE D/A DATA, WITH BIT 0 THE MSB.
;       BITS 14 AND 15 CONTAIN BRIGHTNESS INFORMATION
;       FOR Z-AXIS PULSES. A CLOCK SIGNAL AS SELECTED BY
;       THE DOA INSTRUCTION THEN OUTPUTS THE DATA TO THE
;       SECOND BUFFER AND THE APPROPRIATE DAC.

;DIA:   INPUTS STATUS BITS FROM THE INTERFACE

;D0     1  IF EXTERNAL INTERRUPT REQUEST HAS OCCURRED,
;       0  OTHERWISE
;D1     1  IF DATA READY=1, 0 OTHERWISE.  THIS INDICATES
;          THE PRESENCE OF DIGITAL DATA IN THE FIRST BUFFER.

;D8     1  IF LATE CONVERSION=1, 0 OTHERWISE.  THIS INDICATES
;          A LOSS OF SYCHRONIZATION WITH THE INTERNAL OR
;          EXTERNAL CLOCK IN DATA CHANNEL MODE.

;D15    1  IF /EXTERNAL ERASE INPUT/ LINE IS PULLED LOW,
;       0  OTHERWISE.

;DIB:   INPUTS CURRENT DATA CHANNEL ADDRESS REGISTER

;DIC:   NOT USED
```



```
;11.5   PROGRAM SUBROUTINES:

;11.5.1 INTERRUPT SERVICE ROUTINE:
;THE CALL TO THE INTERRUPT WAIT/SERVICE ROUTINE IS "IWAIT".
;THE ROUTINE WILL WAIT FOR THE TIME SPECIFIED BY THE
;TIMER CONSTANT "DELAY" (300/600 US IN PIO MODE) FOR
;AN INTERRUPT. THE PROGRAM WILL RETURN TO:
; = CALL + 1 IF NO INTERRUPT/UNIDENTIFIED INTERRUPT
; = CALL + 2 IF D/A EXTERNAL INTERRUPT
; = CALL + 3 IF D/A I/O INTERRUPT

;ACCUMULATOR CONTENTS ARE AS FOLLOWS ON RETURN:

;       TYPE            AC0     AC1     AC2
;       ================================
;       NONE            DVC     0       NC
;       UNIDENTIFIED    DVC     BAD     NC
;       D/A EXTERNAL    DVC     DVC     DIA
;       D/A I/O INTR    DVC     DVC     DIA

;WHERE:
;DVC = D/A DEVICE CODE
;BAD = UNIDENTIFIED DEVICE CODE
;NC  = NO CHANGE
;DIA = D/A STATUS WORD
;      BIT 0 = 0 FOR D/A I/O INTERRUPT
;      BIT 0 = 1 FOR D/A EXT INTERRUPT
;      OTHER STATUS BITS ARE
;      BIT 1 = DATA READY
;      BIT 8 = LATE CONVERSION
;      BIT 15 = EXTERNAL ERASE INPUT

;"UNIDENTIFIED INTERRUPT = (##)" IS REPORTED IF
;ANY DEVICE OTHER THAN THE D/A OR TTY IS REQUESTING
;AN INTERRUPT WHERE (##) IS THE INTERRUPTING DEVICE
;CODE. THE ROUTINE WILL ATTEMPT TO CLEAR THE INTERRUPT
;WITH AN 'NIOC' INSTRUCTION ISSUED TO THE DEVICE.

;"EXTERNAL INTERRUPT = (##)" IS REPORTED IF AN
;EXTERNAL INTERRUPT IS REQUESTED FROM THE D/A.
;(##) IS THE D/A DEVICE CODE. IN ADDITION, BIT
;0 OF AC2 SHOULD BE = 1, INDICATING AN D/A
;EXTERNAL INTERRUPT. THE INTERRUPT IS NOT CLEARED.

;TTI/TTO IS HANDLED BY THE DTOS ROUTINE "SWPAK" ON A
;NON-INTERRUPT BASIS. TTI/TTO INTERRUPTS ARE MASKED OUT
;DURING DIAGNOSTIC OPEARTION. THE ONLY EXCEPTION TO THIS
;IS IF THE PAGE ZERO CONSTANT "TTYSW" = -1. IN THIS CASE
;ANY TTI/TTO INTERRUPTS RECEIVED WILL BE CLEARED AND
;CONTROL WILL BE RETURNED TO THE INTERRUPT WAIT LOOP.
;IF "TTYSW" = 0 AND A TTI/TTO INTERRUPT IS RECEIVED,
;IT WILL BE TREATED AS UNIDENTIFIED (THIS INDICATES AN
;ERROR IS THE TTI/TTO INTERRUPT MASK REGISTERS).
```

```
;11.5.2 TTY INPUT/OUTPUT INTERRUPT MASK OUT:
;       THE CALL IS "NOTTY" AND WHEN PERFOMRED, WILL MASK OUT
;       ALL TTY (TTI/TTO) INTERRUPTS. THE INTERRUPT MASK
;       BITS FOR TTI/TTO ARE BITS 14/15 RESPECTIVELY.

;11.5.3 DCH STARTING ADDRESS/WORD COUNT GENERATOR:
;       THE CALL IS "DSAWC".

;       ON RETURN TO CALL + 1:
;       AC0 = DCH RANDOM WORD COUNT (2'S COMPLEMENT)
;       AC1 = DCH RANDOM STARTING ADDRESS
;       AC2 = DCH FINAL ADDRESS (AFTER DCH CYCLE)

;       IF THE SUBTEST ERROR SWITCH IS SET, THEN THE LAST
;       DCH WORD COUNT/STARTING ADDRESS/FINAL ADDRESS BEFORE
;       THE ERROR OCURRED WILL BE RETURNED IN AC'S 0,1 & 2
;       RESPECTIVELY.

;       THE RANDOM STARTING ADDRESSES/WORD COUNTS ARE
;       DETERMINED SUCH THAT NO PROGRAM OR BINARY LOADER
;       DESTRUCTION WILL OCCUR FOR PROPERLY FUNCTIONING
;       DATA CHANNEL LOGIC, NOR WILL CONSOLE DEBUG OPTION
;       OR HAND HELD CONSOLE MEMORY LOCATIONS (077777 -
;       077400) BE ADDRESSED.
```



```
;11.6   D/A CONVERTER SYSTEM MODEL 4224
;       JUMPER CONFIGURATION INFORMATION:

;       JUMPER(S)       FUNCTION/NOTES
;       =========       ==============

;       W1 - W10        D/A CONVERTER RANGE/POLARITY SELECT
;                       FOR CHANNELS "X" & "Y" AS FOLLOWS:

;                                       JUMPERS (INSERTED)
;                       RANGE/POLARITY  DAC "X" DAC "Y"
;                       ==============  ======= =======
;                       +/- 10 VDC      W2,W4   W7,W9
;                       +/- 5 VDC       W2,W5   W7,W10
;                       0 - 5 VDC     W1,W3,W5  W6,W8,W10
;                       0 - 10 VDC      W1,W5   W6,W10

;       W11 - W14       D/A CODING TYPE SELECT AS FOLLOWS:

;                       W11 IN = OFFSET BINARY FOR DAC X
;                       W12 IN = 2'S COMPLEMENT FOR DAC X

;                       W13 IN = OFFSET BINARY FOR DAC Y
;                       W14 IN = 2'S COMPLEMENT FOR DAC Y
;                       (ONLY ONE MAY BE INSERTED FOR EACH).

;       W15 - W20       D/A DEVICE CODE SELECT AS FOLLOWS:

;                       -------- DATA BIT ---------
;                       10   11   12   13   14   15
;                       ---------------------------
;                       W19  W20  W15  W16  W17  W18
;                       DS0 (MSB)               DS5 (LSB)

;                       INSERT CORRESPONDING JUMPER FOR
;                       A "1" IN ANY OF ABOVE DEVICE CODE
;                       SELECT ("DS") BITS.

;       W21, W22      * Z-AXIS PULSE TRIGGERING WHEN DATA
;                       IS LOADED IN CHANNEL "X" OR "Y":

;                       W21 IN = TRIGGER ON DAC "Y" LOAD
;                       W22 IN = TRIGGER ON DAC "X" LOAD
;                       (ONLY ONE MAY BE INSERTED).
;                     * NOTE: D/A MUST BE IN SCOPE MODE.

;       W23 - W26       BRIGHTNESS INFORMATION SELECT FOR
;                       Z-AXIS PULSE AS FOLLOWS:

;                       W23, W24 IN = BRIGHTNESS INFO IN BITS
;                                     14-15 OF DAC X DATA WORD.

;                       W25, W26 IN = BRIGHTNESS INFO IN BITS
;                                     14-15 OF DAC Y DATA WORD.
;                       (ONLY ONE PAIR MAY BE INSERTED).
```

```
;       W27             SELECT WHETHER Z-AXIS PULSE IS
;                       POSITIVE OR NEGATIVE GOING. NO
;                       JUMPER SELECTS NEGATIVE GOING.
;                       W27 IN = POSITIVE GOING. QUIESCENT
;                       DC LEVEL OF Z-AXIS SIGNAL IS SET
;                       BY R27 (SEE BELOW).

;       W28, W29        "DAC DATA VALID" HANDSHAKING SIGNAL
;                       SELECT AS FOLLWS:

;                       W28 IN = TRUE HIGH
;                       W29 IN = TRUE LOW
;                       (ONLY ONE MAY BE INSERTED).

;       W30, W31        "DAC DATA READY" HANDSHAKING SIGNAL
;                       SELECT AS FOLLOWS:

;                       W30 IN = TRUE HIGH
;                       W31 IN = TRUE LOW
;                       (ONLY ONE MAY BE INSERTED).

;       W32             IF INSERTED, A "LATE CONVERSION"
;                       STATUS SIGNAL WILL SET DONE.

;       W33             Z-AXIS COUPLING SELECT AS FOLLOWS:

;                       W33 IN = DC COUPLING ON Z-AXIS
;                       W33 OUT = AC COUPLING ON Z-AXIS

;       D/A CONVERTER POTENTIOMETER INFORMATION:

;       POTENTIOMETER           FUNTION
;       =============           =======

;       R43                     INTERNAL CLOCK FREQUENCY
;                               (NOMINAL RANGE: 16 US - 198 US)
;       R32                     Z-AXIS PULSE LENGTH
;                               (NOMINAL RANGE: 4 US - 158 US)
;       R27                     Z-AXIS DC BASE LEVEL ADJUST
;                               (NOMINAL RANGE +/- 5 VDC)
;       R1                      "X" D/A GAIN ADJUST
;       R2                      "X" D/A OFFSET ADJUST
;       R7                      "Y" D/A GAIN ADJUST
;       R8                      "Y" D/A OFFSET ADJUST
```



```
;11.7   SCOPE LOOP SPEED-UP INFORMATION:

;       TESTS THAT HAVE AN I/O RESET IN THEM (MNRST) USE
;       "L?OPX" (JSR #ICY?C) AS THE SCOPE LOOP HANDLER ROUTINE.
;       WHEN LOOPING ON AN ERROR, THIS ROUTINE ADDS A
;       RATHER LARGE DELAY IN THE SCOPE LOOP IN ORDER TO ALLOW
;       TTY INPUTS TO BE RECOGNIZED AND PROCESSED WITHOUT BEING
;       CLEARED BY THE I/O RESET COMMAND IN THE LOOP. TO SHORTEN
;       THE SCOPE TRACE TIME SIGNIFICANTLY WHEN LOOPING ON AN
;       ERROR OCCURING IN ONE OF THESE TYPE OF LOOPS, SIMPLY
;       CHANGE THE "L?OPX" INSTRUCTION TO A "L?OOP" (JSR #ICYC?E
;       INSTRUCTION. THIS CAN BE DONE BY ENTERING THE OCTAL
;       DEBUG TOOL (ODT). THE CONSTANTS "ICY?C" AND ICYC?E" ARE
;       IN PAGE ZERO. REFER TO THESE LABELS IN THE LISTING TO
;       OBTAIN THEIR RESPECTIVE ADDRESSES FOR THE COMMAND.

;12.    SPECIAL NOTES/SPECIAL FEATURES:
;       ===============================
;       SEE SECTION 8.3 FOR SPECIAL TEST INFORMATION.

;13.    RUN TIME:
;       ========
;       THE FIRST TWO PASSES TAKE APPROXIMATELY 90 SECONDS
;       TO COMPLETE.
```

```
10027 .MAIN
**00000 TOTAL ERRORS, 00000 PASS 1 ERRORS
```